

**REMARKS**

Preliminarily, Applicants request the Examiner to acknowledge and approve the drawings filed on March 27, 2001.

Applicants also thank the Examiner for the telephonic Interview that occurred on December 6, 2004. A Statement of Substance of Interview is filed herewith.

Claims 1-68 are pending in the application. Claims 25-27, 29-32, 64, 65, 67 and 68 are rejected and claims 1-24, 28, 33-63 and 68 have been withdrawn. More specifically, claims 25-27, 29-32, 64, 65, 67 and 68 are rejected under 35 U.S.C. § 103.

Claim 25 has been amended herein. At line 4, the phrase “made of metal and” has been deleted. At the end of the claim, the phrase “wherein the conductor circuit is made of metal” was inserted. Claim 25 was further amended to include the recitation of claim 27 (“wherein each of said first resin insulating layers has a flat and level surface”), which has now been canceled. In addition, several grammatical corrections have been made.

**Brief Summary of the Present Invention**

The present invention relates to a multilayer printed circuit board comprising (1) a resin substrate board having, on both sides thereof, (2) first resin insulating layers each comprised of the same resin material, (3) a lower metal layer, having a conductor circuit made of metal and having the same pattern as said lower metal layer, on each of said first resin insulating layers. The resin insulating layers comprise a thermosetting polyolefin resin. The lower metal layers are composed of at least one metal selected from the group consisting of the metals, not including

Cu, of the 4th through 7th periods in Group 4A through Group 1S of the long-form periodic table of the elements, Al, and Sn.

Figures 19 to 22 illustrate the arrangement of the components of the present invention. As shown in Figure 20(d), the first resin insulating layers 12, which comprise the thermosetting polyolefin resin, are formed on both sides of the resin substrate board 1. The lower metal layer, which may comprise nickel, is formed on each of the first resin insulating layers 12 (*see* Figure 21(a)). The conductor circuit 9 is formed on the lower metal layer (*see* Fig. 21(d)).

As described in the specification at page 54, lines 30 to 33, (*see also* Example 23 and the Figures), the surface of the first resin insulating layer 12 is not roughened. Thus, the lower metal layer is formed on the flat and level surface of the first resin insulating layer 12. *See* currently amended claim 25.

Applicants note that since the lower metal layer is present on the first resin insulating layer, a firm adhesion between the first resin insulating layer 12 and the conductor circuit 9 is obtained without a roughened surface on the first resin insulating layer 12. Applicants further note that since the first resin insulating layers have a flat and level surface, the surface of the conductor circuit is also flat and, as a result, no signal conduction delay occurs even when high-frequency signals are used. *See* page 54, line 33, through page 55, line 2.

**Response to the Rejection of Claims 25-27, 29, 64 and 65 under 35 U.S.C. § 103(a)**

Claims 25-27, 29, 64 and 65 are rejected under 35 U.S.C. § 103(a) as allegedly being unpatentable over EP 743812 to Uno et al. (“Uno”) in view of U.S. Patent No. 4,994,903 to Wroe et al. (“Wroe”).

Applicants respectfully submit that the presently claimed invention is not rendered obvious by the teachings of Uno in view of Wroe.

Uno is directed to a multilayer printed circuit board. As illustrated in Figures 1 to 5 of Uno, the reference teaches a multilayer printed circuit 1, which comprises a substrate 2 having, on both sides, interlaminar resin insulating layers 4. An outer layer copper pattern 6 is formed on each of the interlaminar resin insulating layers 4. The interlaminar resin insulating layer 4 may comprise thermosetting resins such as polyimide resin (*see* page 7, lines 8 to 23) and the outer layer copper pattern 6 may be an electroless copper plated film (*see* page 12, lines 1 to 5). It is noted that the interlaminar resin insulating layer 4 has a roughened surface. *See* page 11, lines 34-36; Figs. 3 and Figs. 5 of Uno.

Wroe is directed to a circuit substrate. As illustrated in Figures 1 and 2, Wroe teaches a substrate 12, a metal layer 30, which comprises a first metal layer 30.1 and a second metal layer 30.5. These layers also correspond to layers 30.6 to 30.8. The second layer 30.5 may comprise copper or aluminum (*see* col. 3, lines 40 to 53). The substrate 12 comprises a electrically insulating layer 24 of organic electrically insulating material, which has a multiplicity of dispersed particles 28. The organic material of the electrically insulating layer 24 may be polyimides or polyolefins (*see* col. 3, lines 8 to 25).

Applicants note that the substrate 2 and the interlaminar resin insulating layer 4 of Uno are roughly analogous to the resin substrate board and the first resin insulating layer of the present invention. Also, the outer layer copper pattern 6 of Uno generally corresponds to the conductor circuit of the present invention.

Applicants submit, however, that Uno fails to teach or suggest the lower metal layer of the present invention. Furthermore, Applicants respectfully submit that the copper layer 6 of Uno does not correspond to the lower metal layer of the present invention.

In the present invention, the lower metal layer is composed of at least one metal selected from among metals (exclusive of Cu) of the 4th through 7th periods in Group 4A through Group 1B of the long-form periodic table of the elements, Al, and Sn. Also, as discussed above, the conductor circuit is formed on the lower metal layer.

According to Uno, however, only the outer layer copper pattern 6 is formed on the interlaminar resin insulating layers 4. Uno does not teach or suggest the formation of an additional conductor layer on the outer layer copper pattern 6.

In Uno, the adhesion between the copper layer 6 and the interlaminar resin insulating layers 4 is poor. Thus, if the copper layer 6 were to be formed on the flat and level surface of the interlaminar resin insulating layers 4, good adhesion could not be obtained. Hence, it is not possible for the copper layer 6 to serve as the lower metal layer of the present invention.

Applicants submit that for these reasons, the outer layer copper pattern 6 of Uno is different than the lower metal layer of the present invention.

Applicants additionally submit that the interlaminar resin insulating layer 4 of Uno does not have a flat and level surface.

Applicants note that Uno clearly indicates that the interlaminar resin insulating layer 4 has a roughened surface 4a (see page 11, lines 34 to 36, and Figure 3). The roughened surface is also shown in Figure 5.

As discussed above, in the present invention, it is not necessary to roughen the surface of the first resin insulating layer, because the lower metal layer on the first resin insulating layer ensures good adhesion between the first resin insulating layer and the conductor circuit. In Uno, however, an interlaminar resin insulating layer with a roughened surface is necessary for good adhesion.

Applicants respectfully submit that Wroe fails to remedy the above-described deficiencies of Uno.

Wroe fails to teach or suggest a metal layer that corresponds to the lower metal layer of the present invention. Furthermore, Wroe does not provide the requisite motivation for modifying the wiring board of Uno in the manner necessary to arrive at the present invention.

In view of the foregoing, Applicants respectfully submit that the rejection of claims 25-26, 29, 64 and 65 should be reconsidered and withdrawn.

**Response to the Rejection of Claims 30-32, 67 and 68 under 35 U.S.C. § 103(a)**

Claims 30-32, 67 and 68 under 35 U.S.C. § 103(a) as allegedly being unpatentable over Uno and Wroe as applied to claim 25 above, and further in view of U.S. Patent No. 5,227,012 to Brandii et al. ("Brandii").

Applicants respectfully submit that claims 30-32, 67 and 68 are not rendered obvious over the teachings of Uno and Wroe in view of Brandii for the same reasons that claims 25-26, 29, 64 and 65 are not rendered obvious over the teachings of Uno and Wroe.

Therefore, it is respectfully submitted that the rejection of claims 30-32, 67 and 68 over § 103 should be reconsidered and withdrawn.

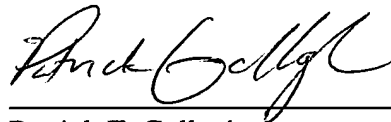
AMENDMENT UNDER 37 C.F.R. § 1.111  
U.S. Application No. 09/806,203

Q63594

In view of the above, reconsideration and allowance of this application are now believed to be in order, and such actions are hereby solicited. If any points remain in issue which the Examiner feels may be best resolved through a personal or telephone interview, the Examiner is kindly requested to contact the undersigned at the telephone number listed below.

The USPTO is directed and authorized to charge all required fees, except for the Issue Fee and the Publication Fee, to Deposit Account No. 19-4880. Please also credit any overpayments to said Deposit Account.

Respectfully submitted,



Patrick F. Gallagher  
Registration No. 54,109

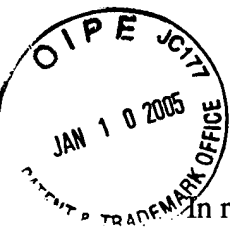
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WASHINGTON OFFICE

**23373**

CUSTOMER NUMBER

Date: January 10, 2005



**PATENT APPLICATION**

**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**

In re application of

Docket No: Q63594

Honchin EN, et al.

Appln. No.: 09/806,203

Group Art Unit: 2814

Confirmation No.: 3753

Examiner: Alonzo Chambliss

Filed: March 27, 2001

For: PRINTED WIRING BOARD AND METHOD FOR PRODUCING THE SAME

**STATEMENT OF SUBSTANCE OF INTERVIEW**

Commissioner for Patents  
P.O. Box 1450  
Alexandria, VA 22313-1450

Sir:

Please review and enter the following remarks summarizing the interview conducted on  
December 6, 2004:

**REMARKS**

An Examiner's Interview Summary Record (PTO-413) was attached with the Office  
communication dated December 15, 2004.

During the interview, the following was discussed:

1. Identification of exhibits or demonstrations: None.
2. Identification of claims discussed: claims 25-27, 29-32, 64, 65, 67 and 68.
3. Identification of art discussed: EP 743812 and U.S. Pat. No. 4,994,903.
4. Identification of principal proposed amendments: None.
5. Brief Identification of principal arguments: Applicants discussed the teachings of  
the prior art with the Examiner.

STATEMENT OF SUBSTANCE OF INTERVIEW  
U.S. Appln. No. 09/806,203

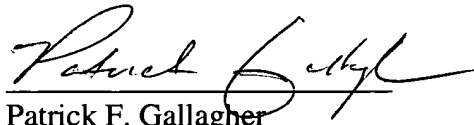
6. Indicaiton of any other pertinent matters discussed: None.

7. Results of Interview: The Examiner agreed to consider Applicants' amendments and arguments when the response is filed.

It is respectfully submitted that the instant STATEMENT OF SUBSTANCE OF INTERVIEW complies with the requirements of 37 C.F.R. §§1.2 and 1.133 and MPEP §713.04.

**It is believed that no petition or fee is required.** However, if the USPTO deems otherwise, Applicant hereby petitions for any extension of time which may be required to maintain the pendency of this case, and any required fee, except for the Issue Fee, for such extension is to be charged to Deposit Account No. 19-4880.

Respectfully submitted,

  
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